REMARKS

This Amendment After Final Rejection under 37 C.F.R. 1.116 is filed in response to the FINAL Office Action mailed on March 18, 2004. All objections and rejections are respectfully traversed.

Claims 1-34 are in the case.

No Claims were added or amended.

At Paragraphs 1-2 of the Office Action claims 1, 7, 11, and 19-21 were rejected under 35 U.S.C. 102 (a) as being anticipated by Greim et al. U.S. Patent 6,163,829 issued December 19, 2000.

Applicants claimed invention, as set forth in representative claim 1, comprises in part:

> 1. A system configured to acknowledge and service an interrupt issued to a processor of an intermediate node, the system comprising:
>
> an external device coupled to a high latency path, the external device generating a pulsed interrupt signal for each type of interrupt supported by the processor;
>
> ***an interrupt multiplexing device accessible by the processor over a fast bus, the interrupt multiplexing device adapted to issue the inter-***

rupt to the processor in response to each pulsed interrupt signal generated by the external device;

a low latency path coupling the external device to the interrupt multiplexing device and adapted to transport each pulsed interrupt signal generated by the external device to the interrupt multiplexing device; and

a status bit stored within the interrupt multiplexing device, the status bit adapted for assertion whenever the pulsed interrupt signal is detected at the interrupt multiplexing device,

wherein the processor efficiently acknowledges the issued interrupt by accessing the interrupt multiplexing device over the fast bus.

Greim discloses an interrupt handler which distributes multiple interrupts among a plurality of processors. Greim's interrupts are received on his external bus (VME bus 12) at VME interface (18), where they are conducted to his interrupt controller (82, Fig. 4) by a bus which has no reference numeral. Interrupt controller (82) is described with reference to Greim's Fig. 6, where interrupts are received on bus 130. Greim's acknowledgements are generated by his interrupt acknowledge box (160), and transmitted back to his VME interface (18) along line (162). The path taken by line 162 is not stated by Greim.

Note that Greim uses the reference numeral "162" for two structures: in his Fig. 6 in the upper right side an "Interrupt Pending Reg."; and his ACK line at the lower right side of his Fig. 6.

Greim's lines 126 are status lines, as explained by Greim at his Col. 29, lines 48-55).

Further, Greim monitors status lines 126, as he explains:

> "The contents of the gating register 122 are compared to the presence of the logic state on the status lines 126 to generate the control bits for the interrupt pending registers 162, the control bits transferred thereto on lines 170. Since the interrupt pending registers 162 have a bit associated with each processor, the interrupt acknowledge block 160 can determine if any of the bits in any of the registers 162 are still set."
> (Col. 29 lines 48-55)

Applicant respectfully urges that Greim is silent concerning Applicant's claimed ***a low latency path coupling the external device to the interrupt multiplexing device and adapted to transport each pulsed interrupt signal generated by the external device to the interrupt multiplexing device***;

Applicant's claim ***a low latency path*** is absent from the disclosure of Greim, as this path would connect Greim's "external device" VME interface (18, Fig. 2) with Greim's interrupt controller (82, Fig. 4). And Greim's only connection is his bus with no reference numeral in his Fig. 4 between his "VME Interface" (18) and his "Interrupt Controller" (82).

In sharp contrast, Applicant, in an exemplary embodiment of the invention, connects his external device "DMA Controller" (550, Fig.. 5) with his "interrupt multiplexing function" field programmable gate array (FGPA) device 560 by "Fast Path 562" (Fig.

5). Greim simply uses his bus with no reference numeral between his VME interface 18 and his interrupt controller 82, and Greim has no fast path connection resembling applicant's claimed novel "Fast Path 562", claimed as Applicant's ***a low latency path coupling the external device to the interrupt multiplexing device and adapted to transport each pulsed interrupt signal generated by the external device to the interrupt multiplexing device.***

Accordingly, Applicant respectfully urges that Greim is legally precluded from anticipating Applicant's claimed novel invention under 35 U.S.C. 102 because of the absence from Greim of Applicant's ***a low latency path coupling the external device to the interrupt multiplexing device and adapted to transport each pulsed interrupt signal generated by the external device to the interrupt multiplexing device*** .

At paragraphs 3-5 of the Office Action claims 2-6 and 12-17 were rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Greim and Shek et al. U.S. Patent No. 6,185,652 issued February 6, 2001.

Applicant respectfully notes that claims 2-6 and claims 12-17 are dependent from independent claims, and the independent claims are believed to be in condition for allowance. Accordingly, the dependent claims are believed to be in condition for allowance.

At paragraph 6 of the Office Action claim 18 was rejected under 35 U.C. 103 (a) as being unpatentable over the combination of Greim, Shek, and Ecclesing U. S. Patent No. 5,983,275 issued November 9, 1999.

Applicant respectfully notes that claim 18 is dependent from an independent claim, and the independent claims are believed to be in condition for allowance. Accordingly, the dependent claims are believed to be in condition for allowance.

At paragraph 7 of the Office Action, claims 8-10 were rejected under 35 U.S.C. 103 (a) as being unpatentable over the combination of Greim and design choice.

Applicant respectfully notes that claims 8-10 are dependent from an independent claim, and the independent claims are believed to be in condition for allowance. Accordingly, the dependent claims are believed to be in condition for allowance.

At paragraph 8 of the Office Action claims 1, 7, and 19-21 were rejected under 35 U.S.C. 103 (a) as being unpatentable over the Swanstrom U. S. Patent No. 5,754,884 issued May 19, 1998, in view of Greim.

Swanstrom discloses a direct memory access DMA controller which services interrupt requests so that while a CPU is servicing one interrupt request the CPU cannot be interrupted by another interrupt request (Col. 10, lines 25-42). The interrupt requests and

corresponding clear actions are transferred over a PCI bus (Col. 11, lines 28-37) and the PCI bus is a preferred embodiment (Col. 11, lines 52-53).

Applicant respectfully urges that Swanstrom is silent concerning Applicant's claimed ***a low latency path coupling the external device to the interrupt multiplexing device and adapted to transport each pulsed interrupt signal generated by the external device to the interrupt multiplexing device***;

Applicant's claimed ***a low latency path*** is absent from the disclosure of Swanstrom, as Swanstrom simply uses a PCI bus to transfer his interrupt requests and clear signals.

In sharp contrast, Applicant, in an exemplary embodiment of the invention, connects his external device "DMA Controller" (550, Fig.. 5) with his "interrupt multiplexing function" field programmable gate array (FGPA) device 560 by "Fast Path 562" (Fig. 5). Swanstrom simply uses his PCI bus, and Swanstrom has no fast path connection resembling applicant's claimed novel "Fast Path 562", claimed as Applicant's ***a low latency path coupling the external device to the interrupt multiplexing device and adapted to transport each pulsed interrupt signal generated by the external device to the interrupt multiplexing device***.

Accordingly, Applicant respectfully urges that Swanstrom and Greim, taken either singly or in combination are legally precluded from anticipating Applicant's claimed novel invention under 35 U.S.C. 103 (a) because of the absence from both Swanstrom and Greim of Applicant's ***a low latency path coupling the external device to the interrupt multiplexing device and adapted to transport each pulsed interrupt signal generated by the external device to the interrupt multiplexing device*** .

At paragraph 9 of the Office Action claims 2-6 and 12-17 were rejected under 35 U.S.C. 103 (a) as being unpatentable over Swanstrom in view of Greim and Shek.

Applicant respectfully notes that claims 2-6 and 12-17 are dependent from an independent claim, and the independent claims are believed to be in condition for allowance. Accordingly, the dependent claims are believed to be in condition for allowance.

At paragraph 10 of the Office Action claims 8-10 were rejected under 35 U.S.C. 103(a) as being unpatentable over the combination Swanstrom, Greim and design choice.

Applicant respectfully notes that claims 8-10 are dependent from independent claims, and the independent claims are believed to be in condition for allowance. Accordingly, the dependent claims are believed to be in condition for allowance.

At paragraph 11 of the Office Action claim 18 was rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Swanstrom, Greim, Shek, and Ecclesine.

Applicant respectfully notes that claim 18 is dependent from an independent claim, and the independent claims are believed to be in condition for allowance. Accordingly, the dependent claims are believed to be in condition for allowance.

At paragraph 12 of the Office Action claims 22-24, 27-29, and 32-34 were rejected under 35 U.S.C. 103(a) as being unpatentable over Swanstrom in view of Greim and Okbay et al. U. S. Patent No. 6,606,677 issued on August 12, 2003.

The invention, as set out in representative claim 22, comprises in part:

> 22. A method for acknowledging and servicing an interrupt issued to a processor, the method comprising:
>
> generating a pulsed interrupt signal at an external device;
>
> ***transporting the pulsed interrupt signal to an interrupt multiplexing device over a first low latency path that couples the external device to the interrupt multiplexing device***;
>
> asserting a status bit in the interrupt multiplexing device corresponding to the interrupt in response to detecting the pulsed interrupt signal;
>
> ***issuing the interrupt to the processor over a second low latency path***;

reading the status bit over the second low latency path by an interrupt handler internal to the processor; and

clearing the status bit in response to the reading of the status bit to effectively ac-knowledge the interrupt.

Okbay discloses an interruptible bridge which interconnects two PCI busses. All interrupt request, and acknowledge, and clear signals apparently pass directly between the two PCI busses and the interruptible bridge. The signals then pass along the PCI busses to the respective processors. The bridge then interrupts the processors by sending signals over the two PCI busses.

Applicant respectfully urges that Okbay is silent concerning Applicant's claimed ***transporting the pulsed interrupt signal to an interrupt multiplexing device over a first low latency path that couples the external device to the interrupt multiplexing device . . . issuing the interrupt to the processor over a second low latency path.***

Applicant's claimed ***low latency path*** is absent from the disclosure of Okbay, as Okbay simply uses a bridge to transfer data between two PCI buses. His two PCI buses are directly connected to his bridge, and so interrupt request, acknowledge, and clear messages are passed between his PCI busses, his bridge, and his CPU. All of Okbay's signals pass along his PCI busses.

In sharp contrast, Applicant, in an exemplary embodiment of the invention, connects his external device "DMA Controller" (550, Fig.. 5) with his "interrupt multiplexing function" field programmable gate array (FGPA) device 560 by "Fast Path 562" (Fig. 5). Okbay simply interconnects his two PCI busses, and Okbay has no fast path connection resembling applicant's claimed novel "Fast Path 562", claimed as Applicant's ***a low latency path coupling the external device to the interrupt multiplexing device and adapted to transport each pulsed interrupt signal generated by the external device to the interrupt multiplexing device***.

Accordingly, Applicant respectfully urges that Okbay, Swanstrom and Greim, taken either singly or in any combination are legally precluded from anticipating Applicant's claimed novel invention under 35 U.S.C. 103 (a) because of the absence from Okbay, Swanstrom, and Greim of Applicant's ***a low latency path coupling the external device to the interrupt multiplexing device and adapted to transport each pulsed interrupt signal generated by the external device to the interrupt multiplexing device*** .

At paragraph 13 of the Office Action claims 25 and 30 were rejected under 35 U.S.C. 103(a) as being unpatentable over Swanstrom, in vies of Greim, Okbay, and Shek.

Applicant respectfully notes that claims 25 and 30 are dependent from independent claims, and the independent claims are believed to be in condition for allowance. Accordingly, the dependent claims are believed to be in condition for allowance.

At paragraph 14 of the Office Action claims 26 and 31 were rejected under 35 U.S.C. 103 (a) as being unpatentable over the combination Swanstrom, Greim, Okbay, Shek, and Ecclesine.

Applicant respectfully notes that claims 26 and 31 are dependent from independent claims, and the independent claims are believed to be in condition for allowance. Accordingly, the dependent claims are believed to be in condition for allowance.

At paragraph 15 of the Office Action, the Examiner responded to Applicant's arguments filed in an earlier Amendment. These arguments are believed to be no longer determinative in view of the absence from all cited art of Applicants claimed novel ***a low latency path coupling the external device to the interrupt multiplexing device and adapted to transport each pulsed interrupt signal generated by the external device to the interrupt multiplexing device*** .

In addition, an analysis under *Graham v. Deere*, 383 U.S. 1, 148 U.S.P.Q. 459, (1966), and cited in MPEP 706.02 (m), comes to the same conclusion, that the claimed

invention is novel and non-obvious. The three analytic criteria under *Graham v. Deer* are:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

Using these analytic criteria, one then makes a legal determination as to whether or not a person of ordinary skill in the pertinent art would have found the claimed invention to be obvious at the time that the invention was made.

First, the scope and content of the prior art is determined by reference to the cited three items: Greim, Swanstrom and Okbay.

The scope and content of the prior art is summarized as:

Greim

Greim discloses an interrupt handler which distributes multiple interrupts among a plurality of processors. Greim's interrupts are received on his external bus (VME bus 12) at VME interface (18), where they are conducted to his interrupt controller (82, Fig. 4) by a bus which has no reference numeral. Interrupt controller (82) is described with reference to Greim's Fig. 6, where interrupts are received on bus 130. Greim's acknow-

ledgements are generated by his interrupt acknowledge box (160), and transmitted back to his VME interface (18) along line (162). The path taken by line 162 is not stated by Greim.

Swanstrom

Swanstrom discloses a direct memory access DMA controller which services interrupt requests so that while a CPU is servicing one interrupt request the CPU cannot be interrupted by another interrupt request. (Col. 10, lines 25-42). The interrupt requests and corresponding clear actions are transferred over a PCI bus (Col. 11, lines 28-37) and the PCI bus is a preferred embodiment (Col. 11, lines 52-53).

Okbay

Okbay discloses an interruptible bridge which interconnects two PCI busses. All interrupt request, and acknowledge, and clear signals apparently pass directly between the two PCI busses and the interruptible bridge. The bridge then interrupts the processors by sending signals over the two PCI busses.

2. The differences between the claimed invention and the cited art are, as set out in the claimed invention: comprises ***a low latency path*** for transferring interrupt acknowledge signals from an ***interrupt multiplexing device*** to an ***external device***. As set out in Claim 1, the difference is that the claimed invention has: ***a low latency path coupling the exter-***

nal device to the interrupt multiplexing device and adapted to transport each pulsed interrupt signal generated by the external device to the interrupt multiplexing device, and this structure is absent from all cited art.

3. The level of ordinary skill in the art of interrupt controllers art can be ascertained by reference to Applicant's Background statement that:

> When the CPU issues a read operation to retrieve the contents of the ISR within the DMA controller to determine the type of interrupt, that read operation also functions to ensure that any pending write operations from the DMA controller to the CPU memory have been "flushed" from those queues. That is, the read operation that informs the CPU as to the type of interrupt generated by the DMA controller also ensures that the data packet and ownership bit transfers have been completed to the CPU memory. In addition, the read operation acknowledges and clears the interrupt at the DMA controller. Thus, the CPU acknowledges and clears the interrupt by retrieving the contents of the ISR in the DMA controller. However, the read operation generally takes a long time to complete because devices coupled to the PCI bus, such as the PCI bridge, need to arbitrate for the shared bus. ***The present invention is directed to reducing the time it takes to acknowledge and clear the interrupt and, in essence, reducing the latency caused by a read operation over a slow bus of the router.*** (Applicant's Specification, Page 4, lines 17-29)

The statement in Applicant's Background Section of his Specification: "***The present invention is directed to reducing the time it takes to acknowledge and clear the interrupt and, in essence, reducing the latency caused by a read operation over a slow***

bus of the router. " indicates that the ordinary level of skill in the art of interrupt handler design has not adequately solved the problem solved by the present invention.

Further, the level of ordinary skill in the art of interrupt handler design can be determined from the cited art, Greim, Swanstrom, and Okbay. In all of these cited patents, the teaching is that persons of ordinary skill in the art have no disclosure of Applicant's claimed novel invention of ***a low latency path***, such as "Fast Path" 552 connecting Applicant's external device to Applicant's interrupt logic "I/O FGPA" 560.

Accordingly, the legal conclusion which is required by the application of the *Graham v. Deere* analytic method, is that a person of ordinary skill in the art of the cited art could not have found the present invention obvious, because of the absence of the claimed elements of the presently claimed invention in all of the cited art.

All independent claims are believed to be in condition for allowance.

All dependant claims are believed to be dependant from allowable independent claims.

The Applicant respectfully solicits favorable action.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,

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